查询S16008LK9供应商

SYNCHRONOUS DRAM

Features:

- Intel PC-100 (3-3-3) or PC133 (3-3-3) compatible
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access precharge time
- Programmable burst lengths: 1, 2, or 4 using Interleaved Burst Addressing
- Auto Precharge and Auto Refresh modes
- 64ms, 4,096-cycle refresh quad-row refresh, (15.6µs/row)
- Self Refresh mode [1]
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- The x16 devices are optimized for both single and dual rank DIMM applications. The x8 devices are optimized for single rank DIMM applications.

Options: Designation:

Family:

SpecTek Memory	SAA

Configuration:

32 Meg x 4 (8 Meg x 4 x 4 banks)	32M4
16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16

Design ID

SDRAM 128 Megabit Design (Call SpecTek Sales for details on availability of "x" placeholders)	Yx5x

Voltage and Refresh:

3.3V, Auto Refresh, 4K refresh	L4
3.3V, Self or Auto Refresh[1], 4K refresh	M4

Package Types:

54-pin plastic TSOP (400 mil)	TK
60-ball FBGA (8mm x 16mm)	FB[2]
60-ball FBGA (11mm x 13mm)	FC[2]

Timing Types:

PC100 (3-3-3)	-8A
PC133 (3-3-3)	-75A

Part number example: SAA16M8Y95AL4TK-75A
(For part numbers prior to December 2004, refer to page 9 for decoding.)

PIN ASSIGNMENT (Top View)

54-Pin TSOP

x4	x8	x16			x16	x8	x4
-	-	VDD	1	54	VSS	-	-
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
-	-	VDDQ	3	52	VSSQ	-	-
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
-	-	VSSQ	6	49	VDDQ	-	-
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
-	-	VDDQ	9	46	VSSQ	-	-
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
-	-	VSSQ	12	43	VDDQ	-	-
NC	NC	DQ7	13	42	DQ8	NC	NC
-	-	VDD	14	41	VSS	-	-
NC	NC	DQML	15	40	NC	-	-
-	-	WE#	16	39	DQMH	DQM	DQM
-	-	CAS#	17	38	CLK	-	-
-	-	RAS#	18	37	CKE	-	-
-	-	CS#	19	36	NC	-	-
-	-	BA0	20	35	A11	-	-
-	-	BA1	21	34	A9	-	-
-	-	A10	22	33	A8	-	-
-	-	A0	23	32	A7	-	-
-	-	A1	24	31	A6	-	-
-	-	A2	25	30	A5	-	-
-	-	A3	26	29	A4	-	-
-	-	VDD	27	28	VSS	-	-

Note: The # symbol indicates signal is active LOW. A dash (–) indicates x8 and x4 pin function is same as x16 pin function.

	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)

NOTES: 1. Only when specified. Consult Sales
2. Not available in x16 configuration

General Description:

The 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. Each is internally configured as a quad-bank DRAM. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered

coincident with the READ or WRITE commands are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, or 4 locations with burst terminate option using the Burst Interleaved Addressing mode only. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving power-down mode. All inputs and outputs are LVTTL-compatible. SDRAMs offer substantial advances in DRAM operating performance, including the abilities to synchronously burst data at a high data rate with automatic column-address generation, to interleave between internal banks in order to hide precharge time, and to randomly change column addresses on each clock cycle during a burst access.

The x8 devices are optimized for single bank DIMM applications. The x16 devices are available for both single and dual bank DIMM applications.

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ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss	-1 to +4.6V
Operating Temperature T_A (Ambient)	25° to +70 °C
Storage Temperature	-55 to +150 °C
Power Dissipation	1 W
Short Circuit Output Current	50 mA

Stresses beyond these may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect reliability.

CAPACITANCE:

Parameter	Symbol	Min	Max	Units
Input Capacitance: A0 - A11, BA0, BA1	C_{I1}	1	5	pF
Input Capacitance: RAS#, CAS#, WE#, DQM, CLK, CKE, CS#	C_{I2}	1	5	pF
Input/Output Capacitance: DQs	C_{IO}	1	6	pF

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter	Symbol	Min	Max	Units
Supply Voltage	Vdd/Vddq	3.0	3.6	V
Input High (Logic 1) Voltage, All inputs	V_{IH}	2.2	Vdd + .3	V
Input Low (Logic 0) Voltage, All inputs	V_{IL}	-0.3	0.8	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd All other pins not under test = 0V	I_I	-10	10	µA
Output Leakage Current DQs are disabled: 0V ≤ VOUT ≤ VddQ	I_{OZ}	-10	10	µA
Output High Voltage (I_{OUT} = -4 mA)	V_{OH}	2.4		V
Output Low Voltage (I_{OUT} = 4 mA)	V_{OL}		0.4	V

ICC OPERATING CONDITIONS AND MAXIMUM LIMITS: Vdd = 3.3V ± 10%V, Temp. = 25° to 70 °C

Supply Current		Symbol	-75A	-8A	Units	Notes
OPERATING CURRENT: ACTIVE mode, burst = 1, READ or WRITE, tRC ≥ tRC (MIN), one bank active, CL=3		Icc1	165	140	mA	1, 2, 3, 4
STANDBY CURRENT: POWER-DOWN mode, CKE = LOW, no accesses in progress	Standard parts	Idd2	9	9	mA	32
	Self refresh parts	Idd2	3	3	mA	32
STANDBY CURRENT: CS# = HIGH, CKE = HIGH, all banks idle		Icc3	75	60	mA	1, 2, 3, 4
STANDBY CURRENT: CS# = HIGH, CKE = HIGH, all banks active after tRCD met, no accesses in progress.		Icc4	75	50	mA	1, 2, 3, 4
OPERATING CURRENT: BURST mode after tRCD met, continuous burst, READ, WRITE, all banks active, CL=3		Icc5	165	145	mA	1, 2, 3, 4
AUTO REFRESH CURRENT tRC ≥ tRC (MIN)	CL = 3	Icc6	265	245	mA	1, 2, 3, 4
AUTO REFRESH CURRENT tRC=15.6us	CL = 3	Icc7	50	50	mA	1, 2, 3, 4
SELF REFRESH CURRENT (Self refresh parts only, part M)		Idd8	3	3	mA	

Notes

1. All voltages referenced to Vss.
2. An initial pause of 100 µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensure. (Vdd and VddQ must be powered-up simultaneously Vss and VssQ must be at the same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
3. Icc specifications are tested after the device is properly initialized. tCK= 10ns for –8 and tCK=7.5ns for –75A.

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AC ELECTRICAL CHARACTERISTICS: Vdd = 3.3V ± 10%V, Temp. = 25° to 70°C

AC CHARACTERISTICS		-75A	-75A	-8A	-8A		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CLK (positive edge) CL = 3	tAC		5.4		6	ns	
Access time from CLK (positive edge) CL = 2	tAC		N/A			ns	
Address hold time	tAH	0.8		1		ns	
Address setup time	tAS	1.5		2		ns	
CLK high level width	tCH	2.5		3		ns	
CLK low level width	tCL	2.5		3		ns	
Clock cycle time CL = 3	tCK	7.5		10		ns	
Clock cycle time CL = 2	tCK	N/A				ns	
CKE hold time	tCKH	0.8		1		ns	
CKE setup time	tCKS	1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time	tCMH	0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time	tCMS	1.5		2		ns	
Data-in hold time	tDH	0.8		1		ns	
Data-in setup time	tDS	1.5		2		ns	
Data-out high impedance time	tHZ		9		9	ns	4
Data-out low impedance time	tLZ	1		2		ns	
Data-out hold time	tOH	2.7		3		ns	
ACTIVE to PRECHARGE command period	tRAS	44	16K	50	16K	ns	
AUTO REFRESH to ACTIVE command period	tRC	60		80		ns	
ACTIVE to READ or WRITE delay	tRCD	22.5		30		ns	
Refresh period (4096 cycles)	tREF		64		64	ms	
PRECHARGE command period	tRP	22.5		30		ns	
ACTIVE bank A to bank B command period	tRRD	15		20		ns	
Transition time	tT	0.3	2	0.3	2	ns	
Write recovery time	tWR	20		20		ns	3
Exit SELF REFRESH to ACTIVE command	tXSR	8		8		tCK	
READ/WRITE command to READ/WRITE command	tCCD	1		1		tCK	1
CKE to clock disable or power down entry mode	tCKED	1		1		tCK	2
CKE to clock enable or power down exit setup	tPED	1		1		tCK	2

AC ELECTRICAL CHARACTERISTICS: Vdd = 3.3V ± 10%V, Temp. = 25° to 70°C

AC CHARACTERISTICS		-75A	-75A	-8	-8		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQM to input data delay	tDQD	0		0		tCK	1
WRITE command to input data delay	tDWD	0		0		tCK	1
Data-in to ACTIVATE command w/ Auto precharge	tDAL	5		5		tCK	3
Data-in to precharge	tDPL	2		2		tCK	2, 3
Last data-in to precharge command	tRDL	2		2		tCK	1
LOAD MODE REGISTER command to command	tMRD	2		2		tCK	1
Data-out to high impedance from precharge	tROH	3		3		tCK	1

NOTES:
1. Clocks required specified by JEDEC functionality and not dependent on any timing parameter.
2. Timing actually specified by tCKS, clock(s) specified as a reference only at a minimum cycle rate.
3. Timing actually specified by tWR plus tRP clock(s) specified as a reference only at a minimum cycle rate.
4. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to Voh or Vol. The last valid data element will meet tOH before going high-Z.
5. Based on tCK = 10ns for –8 and tCK = 7.5ns for –75a

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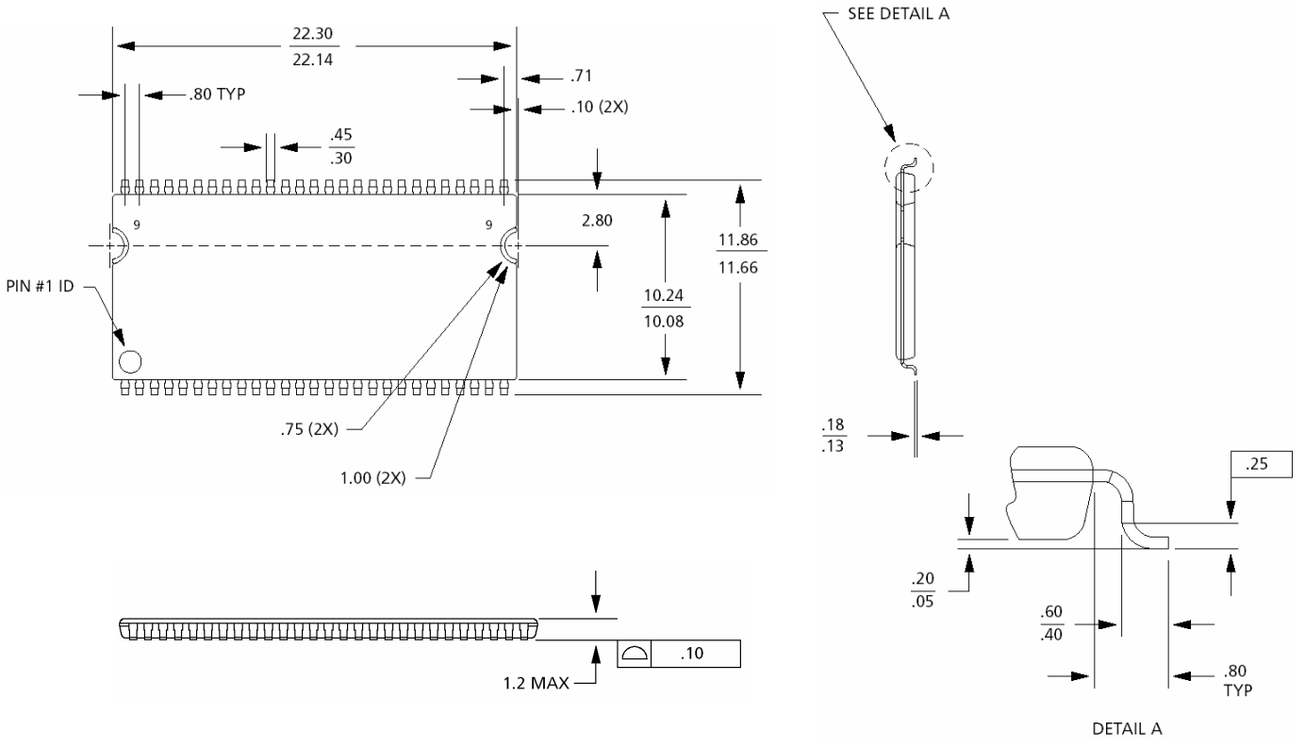
54-PIN PLASTIC TSOP (400 mil)

(Package TK)



NOTE: 1. All dimensions in millimeters MAX/MIN or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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FBGA PIN ASSIGNMENT
(Top View)

32 Meg x 4 SDRAM
11 x 13mm

	1	2	3	4	5	6	7	8
A	NC	VSS					VDD	NC
B	NC	VSSQ					VDDQ	NC
C	VDDQ	DQ3					DQ0	VSSQ
D	NC	NC					NC	NC
E	NC	VSSQ					VDDQ	NC
F	VDDQ	DQ2					DQ1	VSSQ
G	NC	NC					NC	NC
H	NC	VSS					VDD	NC
J	NC	DQM					WE#	CAS#
K	NC	CK					RAS#	NC
L	NC	CKE					NC	CS#
M	A11	A9					BA1	BA0
N	A8	A7					A0	A10
P	A6	A5					A2	A1
Q	A4	VSS					VDD	A3

Depopulated Balls

16 Meg x 8 SDRAM
11 x 13mm

	1	2	3	4	5	6	7	8
A	DQ7	VSS					VDD	DQ0
B	NC	VSSQ					VDDQ	NC
C	VDDQ	DQ6					DQ1	VSSQ
D	DQ5	NC					NC	DQ2
E	NC	VSSQ					VDDQ	NC
F	VDDQ	DQ4					DQ3	VSSQ
G	NC	NC					NC	NC
H	NC	VSS					VDD	NC
J	NC	DQM					WE#	CAS#
K	NC	CK					RAS#	NC
L	NC	CKE					NC	CS#
M	A11	A9					BA1	BA0
N	A8	A7					A0	A10
P	A6	A5					A2	A1
Q	A4	VSS					VDD	A3

Depopulated Balls

8 Meg x 16 SDRAM
11 x 13mm

	1	2	3	4	5	6	7	8
A	DQ15	VSS					VDD	DQ0
B	DQ14	VSSQ					VDDQ	DQ1
C	VDDQ	DQ13					DQ2	VSSQ
D	DQ11	DQ12					DQ3	DQ4
E	DQ10	VSSQ					VDDQ	DQ5
F	VDDQ	DQ9					DQ6	VSSQ
G	NC	DQ8					DQ7	NC
H	NC	VSS					VDD	LDQM
J	NC	UDQM					WE#	CAS#
K	NC	CK					RAS#	NC
L	NC	CKE					NC	CS#
M	A11	A9					BA1	BA0
N	A8	A7					A0	A10
P	A6	A5					A2	A1
Q	A4	VSS					VDD	A3

Depopulated Balls

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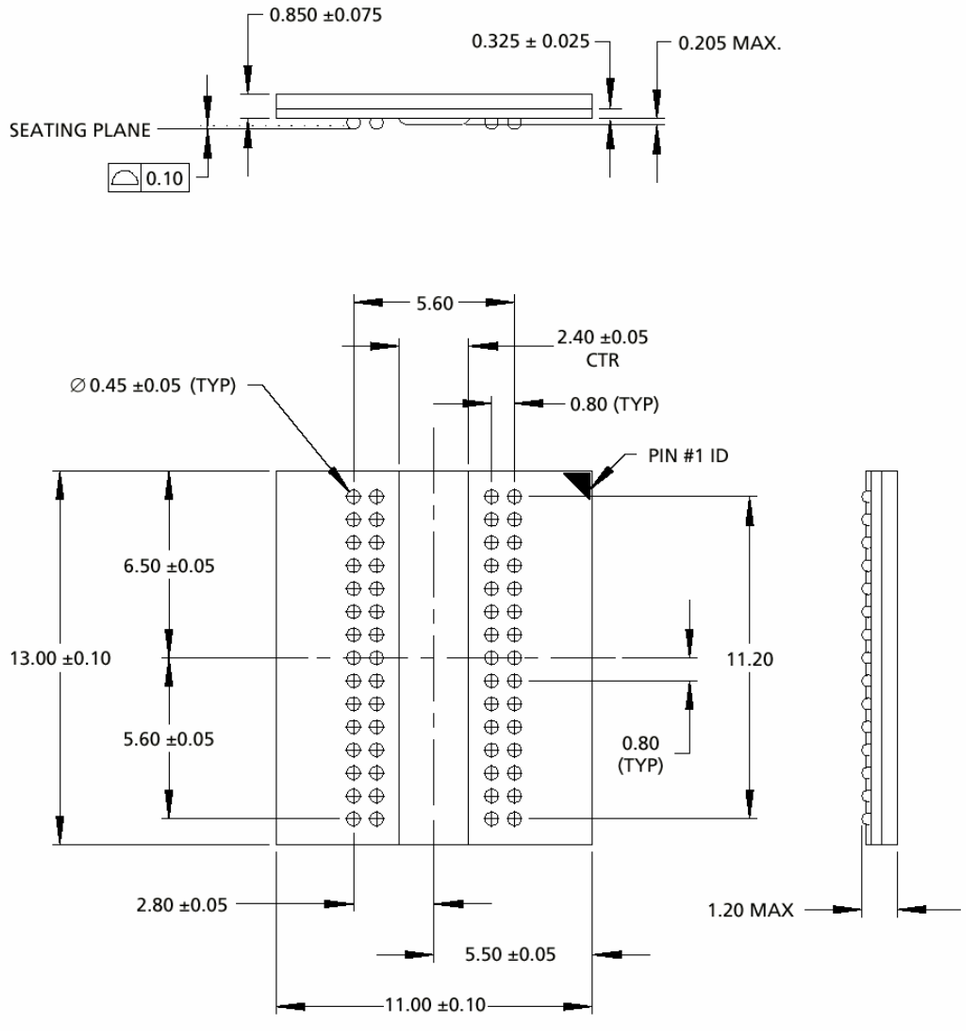
FBGA "FC" PACKAGE
60-pin, 11mm x 13mm



(Bottom View)

NOTE: 1. All dimensions in millimeters.
2. Recommended Pad size for PCB is 0.33mm±0.025mm.

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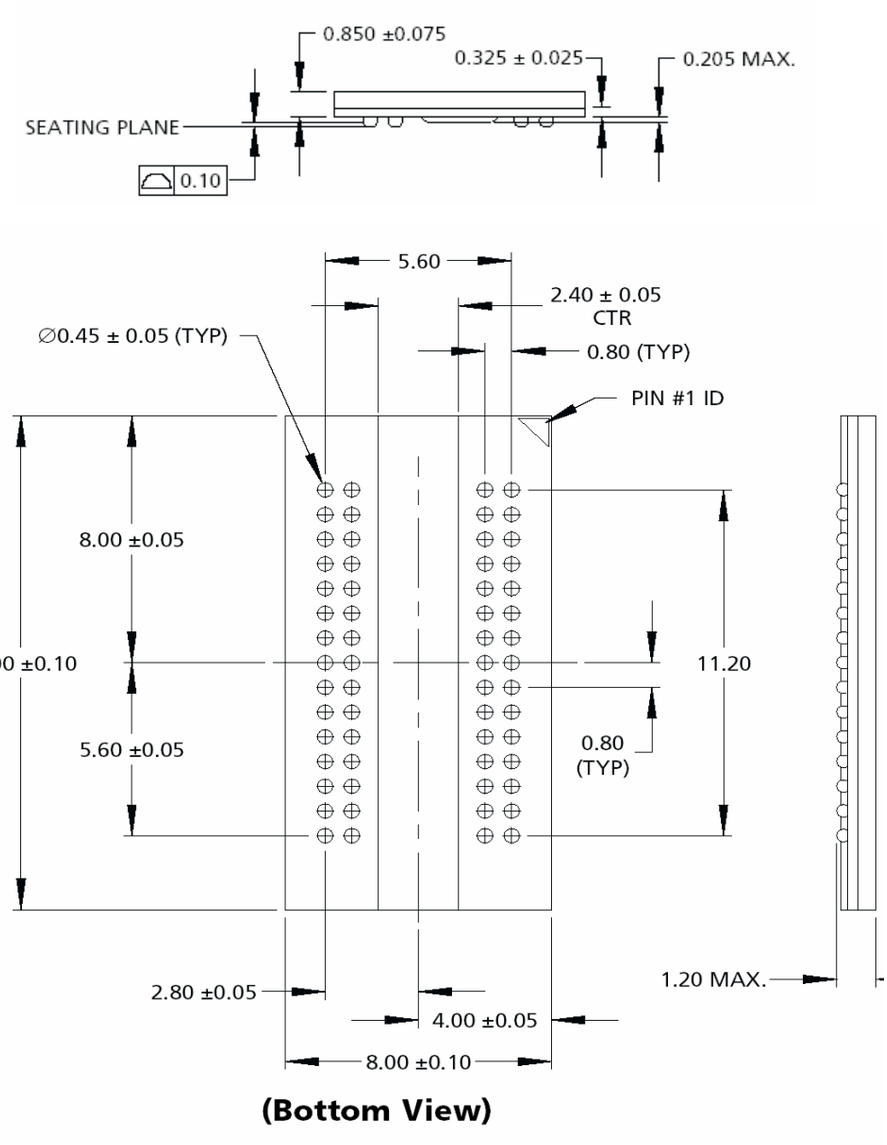
FBGA "FB" PACKAGE
60-pin, 8mm x 16mm



(Bottom View)

NOTE: 1. All dimensions in millimeters.
2. Recommended Pad size for PCB is 0.33mm±0.025mm.

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PART NUMBERS FOR PRODUCT PRIOR TO DECEMBER 2004

Options:	Marking:
Architecture:	
32 Meg x 4 (8 Meg x 4 x 4 banks)	S40032LK8
16 Meg x 8 (4 Meg x 8 x 4 banks)	S80016LK7
8 Meg x 16 (2 Meg x 16 x 4 banks)	S16008LK9
Voltage and Refresh:	
3.3V, Auto Refresh	LK
3.3V, Self or Auto Refresh[1]	MK
Device Configuration:	
32 Meg x 4	8
16 Meg x 8	7
8 Meg x 16	9
Package Types:	
54-pin plastic TSOP (400 mil)	TW
60-ball FBGA (8mm x 16mm)	FB[2]
60-ball FBGA (11mm x 13mm)	FC[2]
Timing Types:	
PC100 (3-3-3)	-8A
PC133 (3-3-3)	-75A

Part number example: S80016LK7TW-8A

NOTES: 1. Only when specified. Consult Sales
2. Not available in x16 configuration

http://www.spectek.com/menus/part_guides.asp

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